TEMIC Status

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Summarize progress made since Jan visit to Nantes:

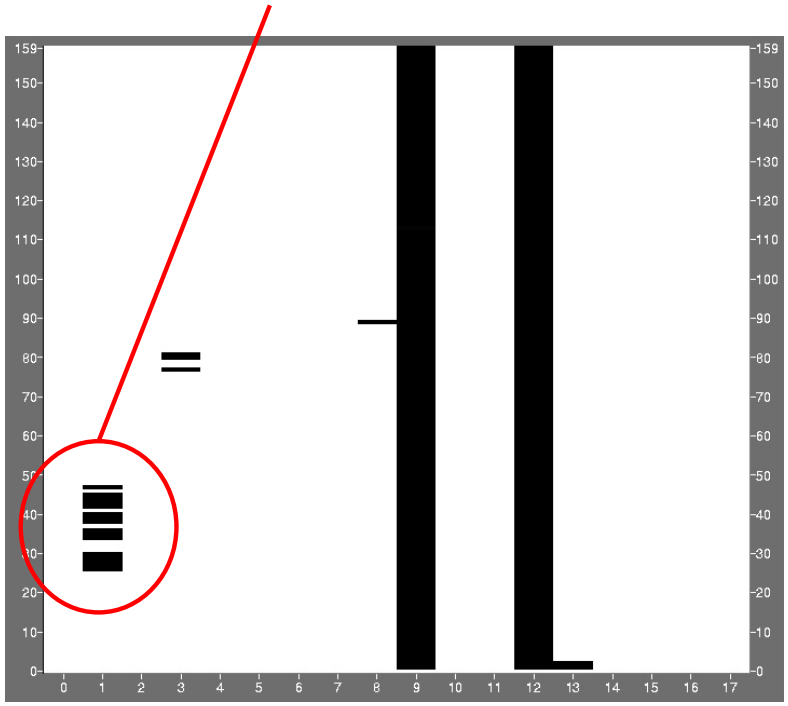
- We completed our program of measurements on FE-D1, including high/low T measurements, and provided all data to TEMIC. We emphasized the problems in the readout logic, which we showed were clearly associated with a leaky NMOS.
- A single chip board with a tested FE-D1 die was sent to TEMIC for analysis.
- There was a long phone conference including TEMIC experts, LETI expert, plus Peter, Laurent, and myself.
- There was a failure hypothesis from R. Truche of LETI (antenna effects)
- We completed first pass at measurements for FE-D1b wafers and single die.
- There was a failure hypothesis from E. Delagne of Saclay.

Reverse Engineering of FE-D Die

First characterized a chip, locating bad pixels:

First Chip: FED #6:

THIS CHIP HAS A CLUSTER OF BAD PIXELS IN COLUMN 1:



PIXEL ID	20MHz READOUT	20MHz FREEZE	10MHz READOUT	10MHz FREEZE	5MHz READOUT	5MHz FREEZE
26 (BAD)	OK	OK	OK	OK	DEAD	OSCIL
27 (BAD)	ROW-0	OSCIL	DEAD	OSCIL	DEAD	OSCIL
28 (BAD)	OK	OK	EXCESS	OSCIL	DEAD	OSCIL
29 (BAD)	OK	OK	ROW-0	OSCIL	DEAD	OSCIL
30 (BAD)	DEAD	OSCIL	DEAD	OSCIL	DEAD	OSCIL
31 (BAD)	OK	OK	OK	OK	DEAD	OSCIL
32 (BAD)	OK	OK	OK	OK	DEAD	OSCIL
33 (GOOD)	OK	OK	OK	OK	OK	OK
34 (BAD)	OK	OK	DEAD	OSCIL	DEAD	OSCIL
35 (BAD)	DEAD	OSCIL	DEAD	OSCIL	DEAD	OSCIL
36 (BAD)	ROW-0	OSCIL	DEAD	OSCIL	DEAD	OSCIL
37 (BAD)	OK	OK	OK	OK	50%	OSCIL
38 (BAD)	DEAD	OSCIL	DEAD	OSCIL	DEAD	OSCIL
39 (BAD)	OK	OK	ROW-0	OSCIL	DEAD	OSCIL
40 (BAD)	OK	OK	ROW-0	OSCIL	DEAD	OSCIL
41 (GOOD)	OK	OK	OK	OK	OK	OK
42 (BAD)	OK	OK	ROW-0	OSCIL	DEAD	OSCIL
43 (BAD)	ROW-0	OSCIL	DEAD	OSCIL	DEAD	OSCIL
44 (BAD)	OK	OK	DEAD	OSCIL	DEAD	OSCIL
45 (BAD)	OK	OK	DEAD	OSCIL	DEAD	OSCIL
46 (GOOD)	OK	OK	OK	OK	OK	OK
47 (BAD)	EXCESS	OSCIL	DEAD	OSCIL	DEAD	OSCIL

- Digital scans gave a cluster of bad pixels, then individual probing was used to classify their behavior as a function of the column clock frequency.

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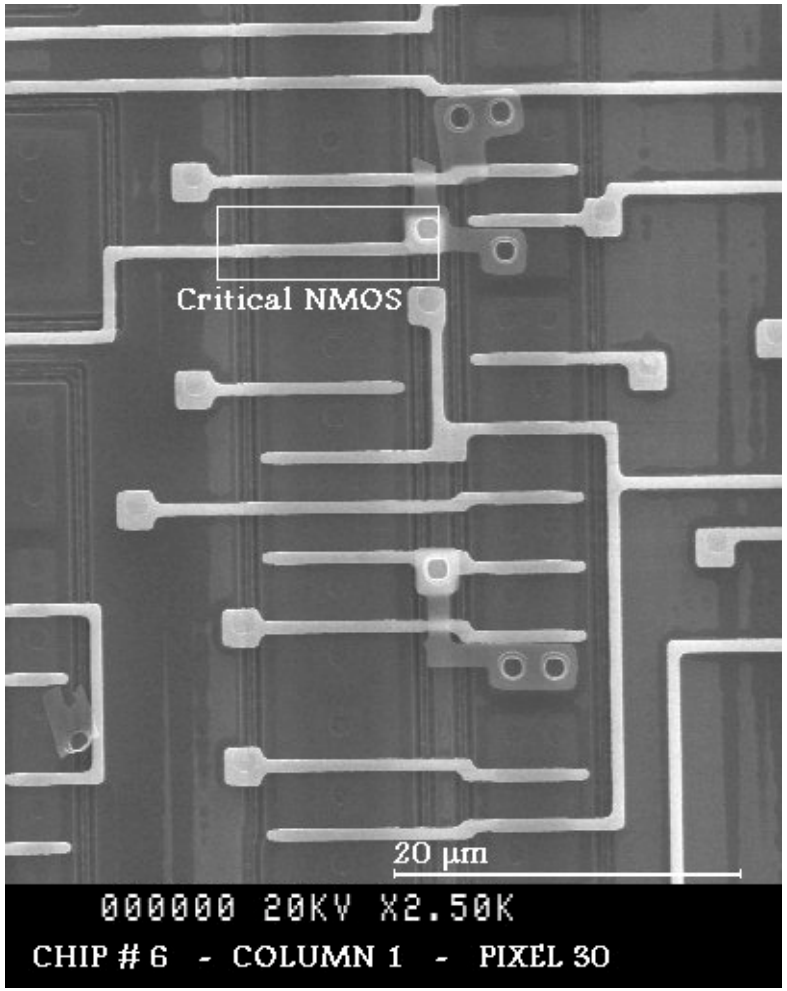
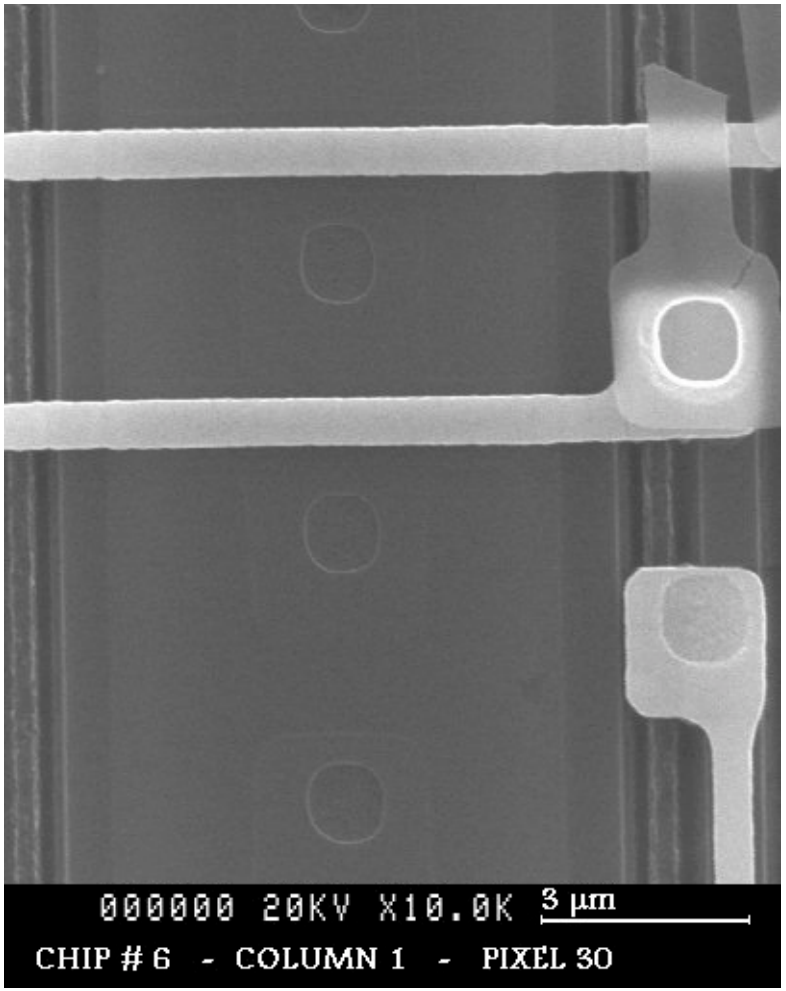
- TEMIC then reverse engineered (removed layers by chemical etch steps) to explore whether there were problems in the poly patterning step:





- Box surrounds gate of reset NMOS (leaky device). Figure on right shows expanded view of gate, and also nearby M1-poly contacts overlapping trenches.

Conclusions:

- No sign of any problems in poly patterning.

Phone Conference (April 27):

- Thierry Corbiere arranged a long phone conference with TEMIC process expert (Christian Lemouellic), LETI process expert (Robert Truche), and LArg DMILL expert (Eric Delagne).
- We briefly summarized out measurements of FE-D1. Concern among experts of the complexity of interpreting the results of our I/V measurements “in situ”.
- Eric described the LArg problem in their recent SCA submission (anomalous leakage in their analog memory cells). This was traced to a problem with placing M1-poly contacts or parallel poly traces over a trench (edge of GENNMOS or GENPMOS layer), with close spacing. This is allowed by the DRC, but can cause difficulties with the poly etch.
- Laurent summarized the problems CPPM had with the two versions of the MAREBO fabricated by TEMIC, also involving leakage problems with dynamic logic. Laurent suggested the possibility of direct leakage from inside trenches to lost silicon as a possible mechanism.
- Robert mentioned their suspicion that the problem could be related to damage to the gate oxide during fabrication due to antenna effects.

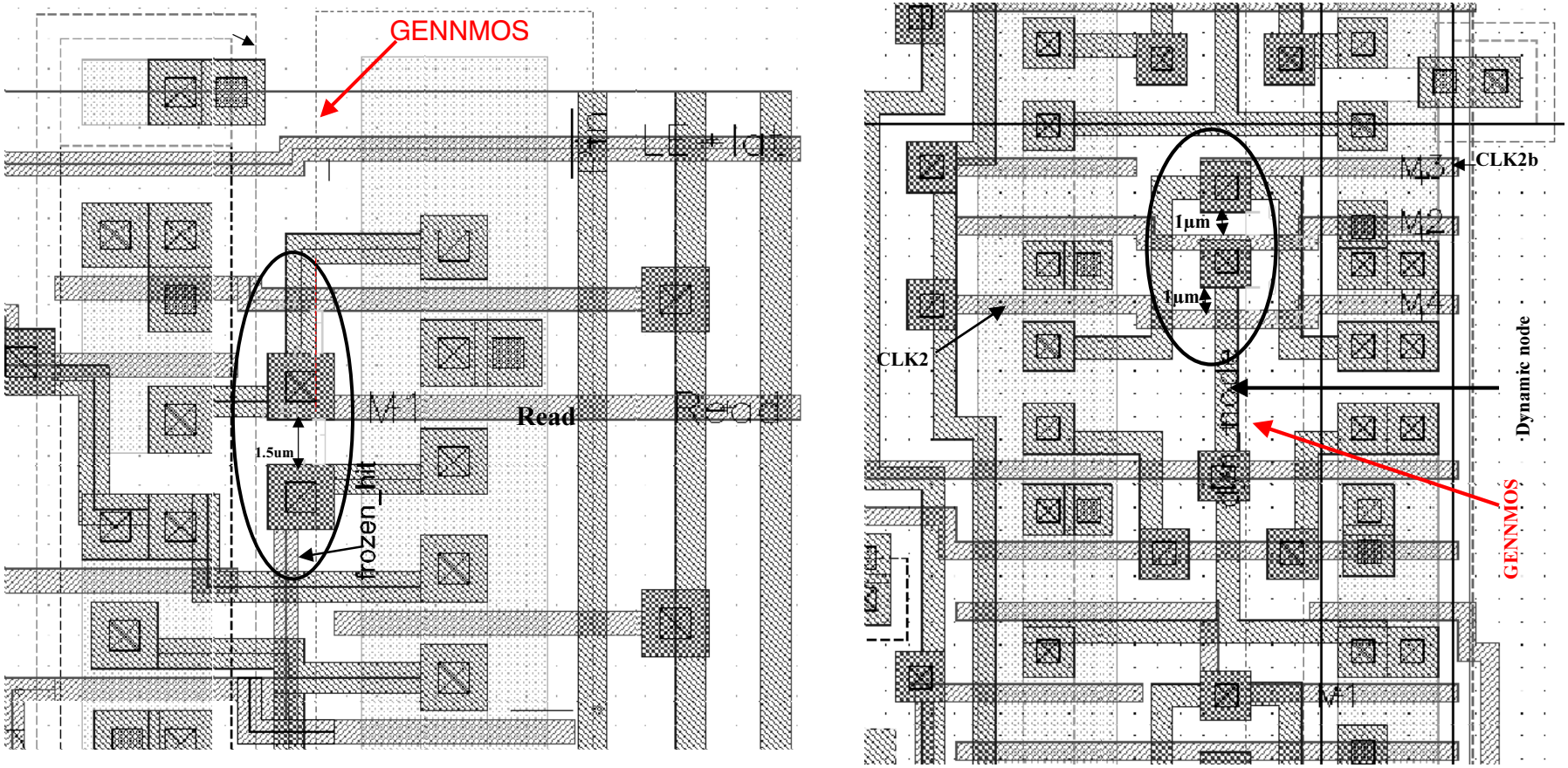
- Another feature of our layout is the very large wells used within the active area (the pixel hit logic for each pixel sits inside a well which extends the full 8mm length of the column).

Follow up:

- LETI examined our layout in more detail, and suggested to TEMIC to pursue further understanding of the antenna effect problem.
- In brief, this is a damage mechanism for the gate oxide during fabrication. It occurs when there are large aspect ratio conductors attached to floating gates. A ratio is calculated of the area of the conductor (poly or M1) to the floating gates. In DSM processes, this ratio is typically limited to less than 100-200. In our column pair, the long control busses (8000μ x 1.6μ) are always connected to a large number of floating gates (typically at least 160 min size devices, 2.2μ x 0.8μ), giving ratios of 50 or less.
- Eric Delagne was provided with GDS files and schematics for the problem areas of FE-D (the pixel register and the hit logic).
- He performed a detailed analysis, and sent us a memo summarizing his results.
- The effect he was predicting should have appeared in the TEMIC reverse engineering analysis. In addition, the agreement with our understanding of FE-D1 is not completely consistent...

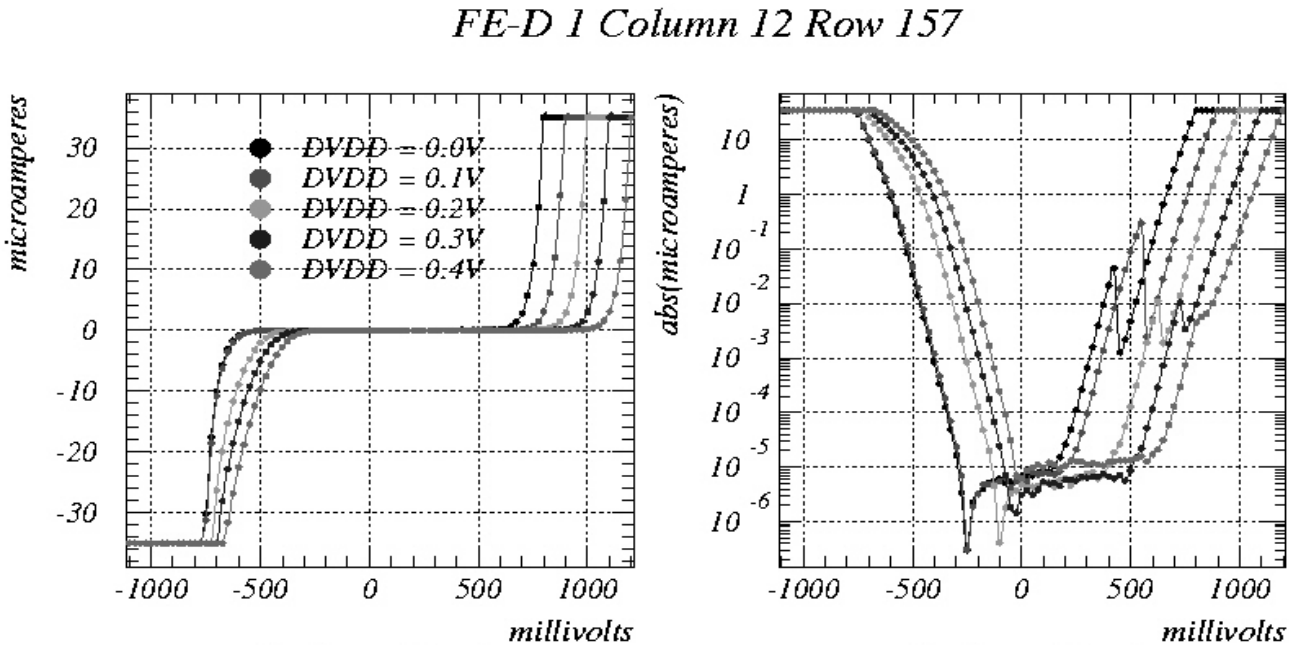
Eric Delagne analysis:

- After a detailed study, Eric concluded that in his opinion, the problem with traces and contacts over trenches could also be at the root of the FE-D problems. In particular, for the two low-yield logic blocks, he indicated the following:



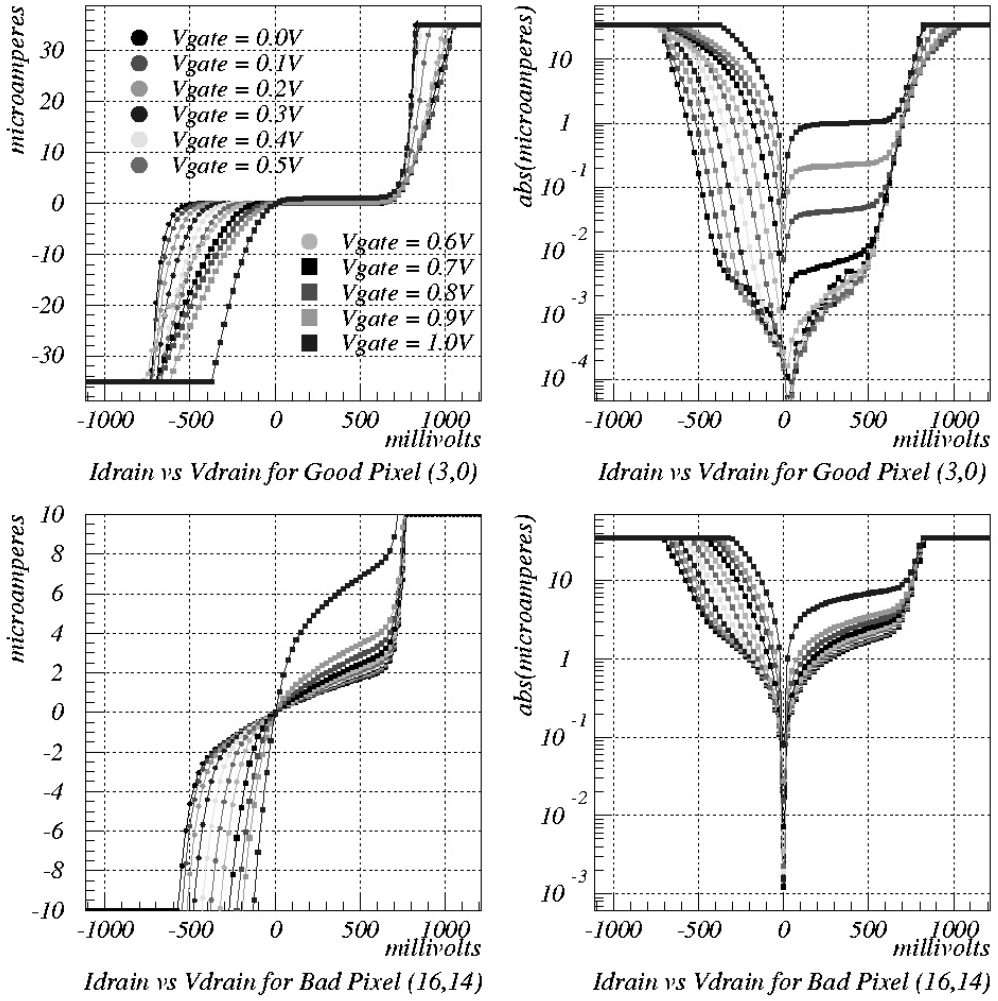
- Left is the hit logic, with R between Read and FrozenHit, right is Pixel Register.

- After we examined the FE-D1 layout in more detail, it was clear that there was a strong correlation between layout features of this type, and dynamic nodes with/ without problems.
- In particular, there is no such layout feature in the LE/TE RAM (where we see no evidence of defects, despite the fact there are 14 bits per pixel, compared to the one dynamic node in the hit logic), nor in the ff_edge FF in the hit logic, nor in the ff_edge FF in the EOC blocks.
- In addition, Mario has studied whether this type of problem could explain the mysterious “diode shift” which we observe in all devices. He believes it could be consistent, since even large resistances could cause diode shifts, whereas small resistances are required to actually cause the “row 0” failure we see:



- Diode being turned on for negative VDrain is from drain implant to well, connected to DGND. It should not move when DVDD is varied.

- On the other hand, this model makes detailed predictions for failures, including that the hit logic failure should appear as a resistance between the FrozenHit and the Read node (the drain and the gate of the leaky NMOS). In our detailed measurements from LBL (made at Peter's suggestion), we can rule this out:



- If the resistance was between drain and gate, then in this series of 2D scans, the curves would not always pass through zero current when the drain voltage was zero. Instead, they would shift so that zero current occured when the drain-gate voltage was zero.

Conclusions:

- We will continue to discuss these issues with relevant experts.
- Mario has tried to respect Eric's proposed "extended DRC" to reduce probability of problems with poly etching, although the details of this picture do not completely match our results.

FE-D2 run:

- We have proposed to TEMIC, based in part on strong suggestion from LETI, that the next engineering run should not be a standard run.
- Instead, we would like to get immediate delivery on the full complement of wafers started (16-20).
- In addition, we have requested that TEMIC, in consultation with LETI, should include some "technology splits" in this run, to divide the wafers into two or four subgroups, each processed in a slightly different way. Example might include change of poly etch from normal. We would analyze all of these wafers and provide feedback to TEMIC on yield.
- This proposal was first discussed over one month ago, and as of this moment, we have no response from TEMIC on whether or not they are willing to do this.
- If not, propose to proceed with standard run, and depending on results, this would be the last run with TEMIC for FE chips.